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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte DAVID ROBERT BALDWIN

Appeal 2009-003677
Application 09/591,225
Technology Center 2600

Decided: August 28, 2009

Before MAHSHID D. SAADAT, KARL D. EASTHOM, and ELENI MANTIS MERCEDER, *Administrative Patent Judges*.

EASTHOM, *Administrative Patent Judge*.

DECISION ON APPEAL

STATEMENT OF THE CASE

Appellant appeals under 35 U.S.C. § 134(a) from the Examiner's final rejection of claims 1-5, 7-10, and 12-22 (App. Br. 6).[1] We have jurisdiction under 35 U.S.C. § 6(b).

We affirm-in-part.

Appellant's invention provides a graphics processor that accesses a host processor memory in the event of a page fault, without involving the host processor (Spec. 8:11 to 9:1).

Claim 1, illustrative of the invention, follows:

1. A computer system, comprising:
a graphics accelerator unit which manages page faulting of texture data invisibly to the host processor.

The Examiner relies on the following prior art references:

Kaiser EP 0766177 A1 Feb. 4, 1997

James F. Blinn, *The Truth About Texture Mapping*, IEEE Computer Graphics and Applications, 78-83 (1990).

The Examiner also relies on the following evidentiary reference:

Tim Brecht, *Nachos Assignment # 3: Caching TLB's and Virtual Memory*, avail. at http://www.cs.uwaterloo.ca/~brecht/courses/4321/handouts/vm.ps (*hereinafter* "Nachos.")[2]

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[1] Appellant's Brief (filed July 19, 2007) ("App. Br.") and Reply Brief (filed Oct. 26, 2007) ("Reply Br."), and the Examiner's Answer (mailed Sept. 26, 2007) ("Ans."), detail the parties' positions and are referenced in this opinion.

[2] This reference "Due date" is listed as Nov. 11, 1997 on its first page. Appellant does not contest the prior art status of the document. The
Footnote continued on the next page.

The Examiner rejected:

Claims 1-5, 7-10, and 12-22 under 35 U.S.C. § 103 based upon Kaiser and Blinn.

ISSUE

Appellant and the Examiner dispute the meaning of the term "page fault." The arguments and rejections present the following issue:

Did Appellant demonstrate that the Examiner erred in finding that Kaiser's TLB misses constitute page faults such that Kaiser discloses "a graphics accelerator unit which manages page faulting of texture data invisibly to the host processor" as recited in claim 1?

FINDINGS OF FACT (FF)

Kaiser distinguishes a page fault from a TLB (translation lookaside buffer) miss (col. 5, l. 45 to col. 6, l. 2). Kaiser describes host processor involvement during a page fault as follows:

> Since memory controller 204 is not a processor, it cannot deal directly with a page fault. If a page fault condition occurs while graphics processor 206 is processing a command block from the main processor complex 12, an error status packet reflecting the page fault condition is passed to the processor 12 by memory controller 204.

(Kaiser, col. 6, ll. 3-9).

Examiner also refers to another website (Ans. 5) which further describes the Nachos computer system described in the Nachos document.

PRINCIPLES OF LAW

"[T]he examiner bears the initial burden, on review of the prior art or on any other ground, of presenting a *prima facie* case of unpatentability." *In re Oetiker*, 977 F.2d 1443, 1445 (Fed. Cir. 1992). "[T]here must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness." *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006). "'On appeal to the Board, an applicant can overcome a rejection by showing insufficient evidence of *prima facie* obviousness . . . .'" *Id.* at 985-86 (*quoting In re Rouffet*, 149 F.3d 1350, 1355 (Fed. Cir. 1998).

During examination of a patent application, the PTO "is obligated to give claims their broadest reasonable interpretation during examination." *In re Am. Acad. Of Sci. Tech. Ctr.*, 367 F.3d 1359, 1369 (Fed. Cir. 2004). "[T]he words of a claim 'are generally given their ordinary and customary meaning.'" *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312 (Fed. Cir. 2005) (en banc) (internal citations omitted). "'[C]laims must be construed so as to be consistent with the specification, of which they are a part.'" *Id.* at 1316 (citation omitted).

ANALYSIS

Appellant, focusing on claim 1, contends (App. Br. 12) that "Kaiser explicitly requires the host processor to handle a page fault." The Examiner (Ans. 3-6) does not dispute this contention which the record supports (FF), but rather, contends that in Kaiser, a TLB miss, which does not involve host processor action, constitutes a page fault. The Examiner cites a web based "Nachos" document and a supporting document (*see supra* note 2) as evidence to show that skilled artisans refer to such a TLB miss as

a page fault. The Examiner states (Ans. 5-6): "This reference more clearly shows that a TLB miss is considered a 'page fault' even when the operating system then checks its page table."

Appellant disputes (App. Br. 13-14) the Examiner's reasoning, first emphasizing that Kaiser (FF) and Appellant differentiate between a page fault and a TLB miss. Appellant also contends (App. Br. 13) that Kaiser's "definition of a page fault is common and well established," and like Appellant's Specification, involves a "second level of memory (i.e. the host's physical memory)." The Examiner's assertions notwithstanding, on balance, the Nachos document (and its supporting document cited by the Examiner) does not refute Appellant's contention.

Appellant argues that a TLB miss in Nachos is different than the TLB miss in Kaiser. Appellant explains (App. Br. 16) that the difference in terminology occurs "for two reasons: first, because Nachos itself is the host, and second, because Nachos replaces the Nachos (host) page table with a TLB." As Appellant points out (App. Br. 17), the Examiner "does not characterize Nachos as teaching page faults without host processor involvement" (*see* Ans. 5). In other words, the Examiner does not refute Appellant's contention that a host processor is involved in the page fault of Nachos. As such, Appellant's arguments demonstrate that while the skilled artisans may interpret a TLB miss with host processor involvement as a page fault, the Examiner has not established that without such involvement (as called for in the claims and disclosed by Appellant), skilled artisans would so interpret a TLB miss.

The Examiner's comparison (Ans. 4) of Appellant's Specification to Kaiser also does not support the finding that Kaiser meets the disputed

limitation of claim 1. Specifically, the Examiner's comparison of an address miss in the Specification to that in Kaiser does not point to any description in Appellant's Specification, nor does it articulate in terms of a second level of memory as set forth in Appellant's Specification relating to a page fault, sufficiently to demonstrate how Kaiser's TLB address miss encompasses a page fault (*see* Ans. 4). Therefore, Appellant has established that the Examiner erred in determining that skilled artisans, in light of the Specification, would have understood Kaiser's TLB miss to include a page fault as required by claim 1.

Accordingly, we will not sustain the Examiner's rejection of claim 1, which recites "a graphics accelerator unit which manages page faulting of texture data invisibly to the host processor." For similar reasons, we will not sustain the Examiner's rejection of claims 2, 3, 8, 9, 10, 12-15, and 21, which recite similar limitations.

On the other hand, while Appellant asserts (App. Br. 14) that "[v]arious claims of the present application claim no host processor involvement in a page fault (e.g., texture data is fetched 'automatically' or 'invisibly' to the host processor)," claims 4, 5, 7, and 16-20 do not recite any such "page fault" limitation, nor any management thereof as invisible to the host processor. While claim 22 recites "page faulting," the claim does not require management thereof as invisible to the host processor (or any similar limitation as argued). Accordingly, we will sustain the Examiner's rejection of these claims.

CONCLUSION

Appellant demonstrated that the Examiner erred in finding that Kaiser's TLB misses constitute page faults and that Kaiser discloses "a graphics accelerator unit which manages page faulting of texture data invisibly to the host processor" as recited in claim 1.

DECISION

We reverse the Examiner's decision rejecting claims 1-3, 8-10, 12-15 and 21. We affirm the Examiner's decision rejecting claims 4, 5, 7, 16-20, and 22.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv).

AFFIRMED-IN-PART

tkl

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